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**PATENT NUMBER and  
ISSUE DATE**

**U.S. UTILITY Patent Application**

APPL NUM 10015209	FILING DATE 11/16/2001	CLASS 438	SUBCLASS 1	GAU 2825	EXAMINER - THOMPSON
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**\*\*APPLICANTS:** Hashimoto Eiki;

**\*\*CONTINUING DATA VERIFIED:**

*None* *[Signature]*

**\*\* FOREIGN APPLICATIONS VERIFIED:**

JAPAN 354306/2000 11/21/2000 *VERIFIED* *[Signature]*

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	
Foreign priority claimed 35 USC 119 conditions met Verified and Acknowledged Examiners's initials		Yes <input type="checkbox"/> no <input checked="" type="checkbox"/> Yes <input type="checkbox"/> no <input checked="" type="checkbox"/>	ATTORNEY DOCKET NO NEKU 19.181
TITLE : Semiconductor circuit designing apparatus and a semiconductor circuit designing method in which the number of steps in a circuit design and a layout design is reduced			
U.S. DEPT. OF COM. IDA 20101 DTD 12/26/01 10:20 AM			

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Total Claims	Print Claim for 10.0
Assistant Examiner		DRAWING	
		Sheets Drawn	Fig.s Drawn
Primary Examiner		Print Fig.	
		Application Examiner	
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